HGD050N10A P-1

100V N-Ch Power MOSFET

Feature

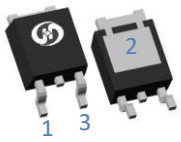
◇ High Speed Power Switching
◇ Enhanced Body diode dv/dt capability
◇ Enhanced Avalanche Ruggedness
◇ 100% UIS Tested, 100% Rg Tested
◇ Lead Free

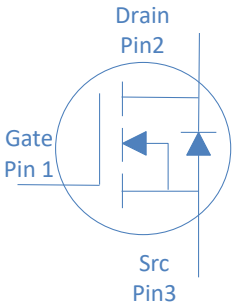
Application

◇ Synchronous Rectification in SMPS
◇ Hard Switching and High Speed Circuit
◇ Power Tools
◇ UPS
◇ Motor Control

V_{DS}		100	V
$R_{DS(on),typ}$	V_{GS}=10V	4.8	mΩ
$I_{D\ (Sillicon\ Limited)}$		115	A

TO-252





Part Number	Package	Marking
HGD050N10A	TO-252	GD050N10A

Absolute Maximum Ratings at T_j=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	115	A
		T_C=100℃	81	
Drain to Source Voltage	V_{DS}	-	100	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	400	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25℃	80	mJ
Power Dissipation	P_D	T_C=25℃	150	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to175	℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\Theta JC}$	1	℃/W
Thermal Resistance Junction-Ambient	$R_{\Theta JA}$	46	℃/W

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	2	3	4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=100V, T_j=25℃	-	-	1	μA
		V_{GS}=0V, V_{DS}=100V, T_j=100℃	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	4.8	5.3	mΩ
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	60	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	1.2	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=50V, f=1MHz	-	3490	-	pF
Output Capacitance	C_{oss}		-	571	-	
Reverse Transfer Capacitance	C_{rss}		-	18	-	
Total Gate Charge	Q_g	V_{DD}=50V, I_D=20A, V_{GS}=10V	-	47	-	nC
Gate to Source Charge	Q_{gs}		-	10	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	10	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=50V, I_D=20A, V_{GS}=10V, R_G=10Ω,	-	12	-	ns
Rise time	t_r		-	7	-	
Turn off Delay Time	$t_{d(off)}$		-	25	-	
Fall Time	t_f		-	5	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=50V, I_F=20A, dI_F/dt=500A/μs	-	50	-	ns
Reverse Recovery Charge	Q_{rr}		-	350	-	nC

Fig 1. Typical Output Characteristics

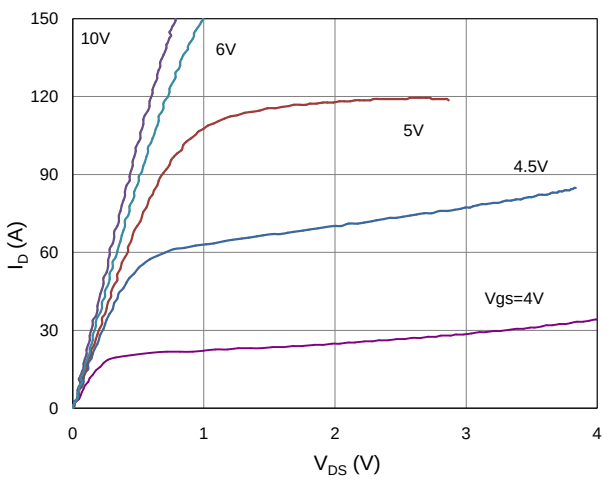


Figure 2. On-Resistance vs. Gate-Source Voltage

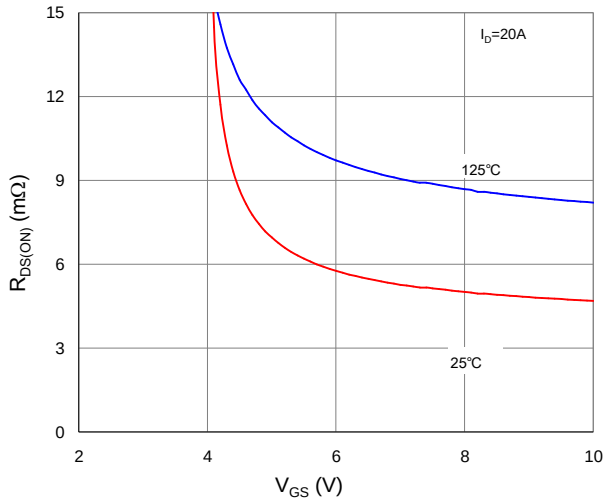


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

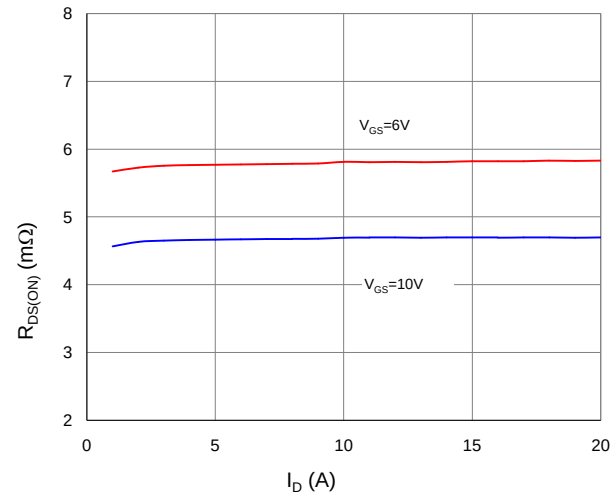


Figure 4. Normalized On-Resistance vs. Junction Temperature

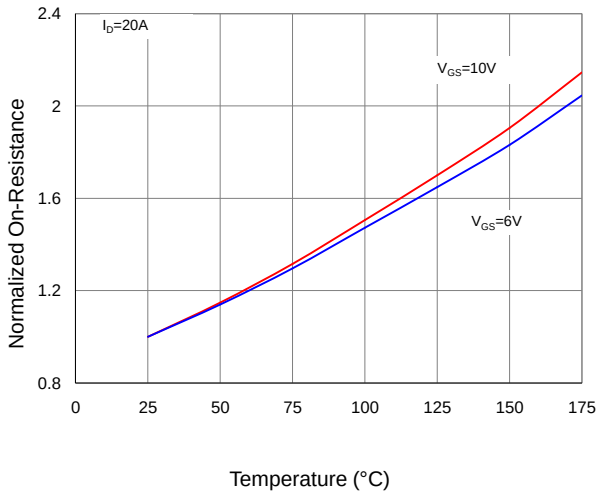


Figure 5. Typical Transfer Characteristics

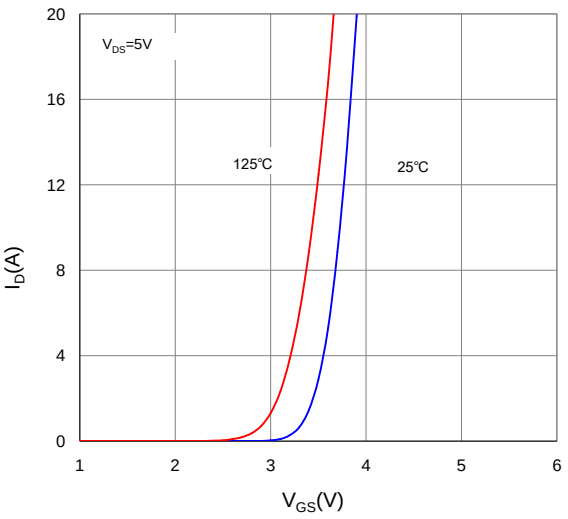


Figure 6. Typical Source-Drain Diode Forward Voltage

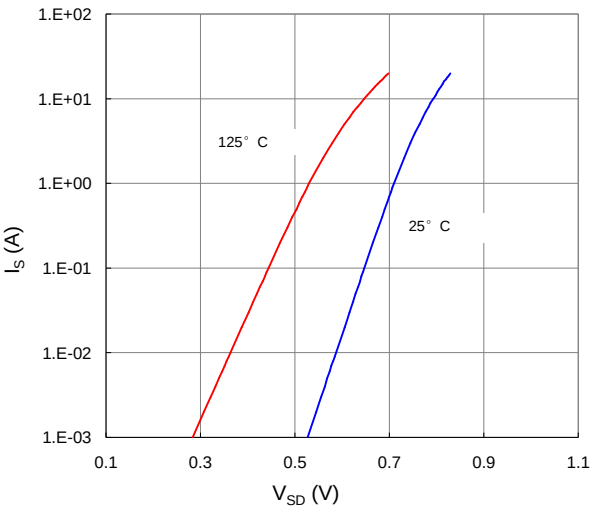


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

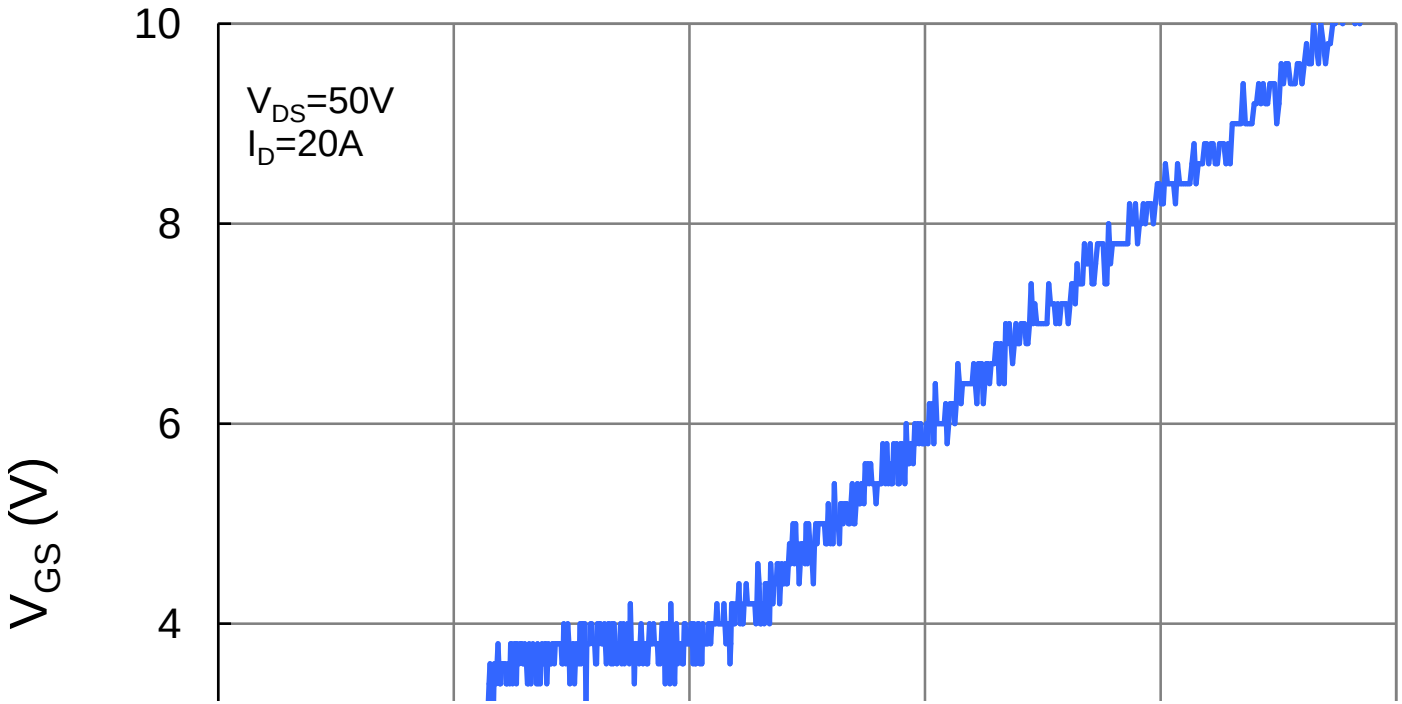
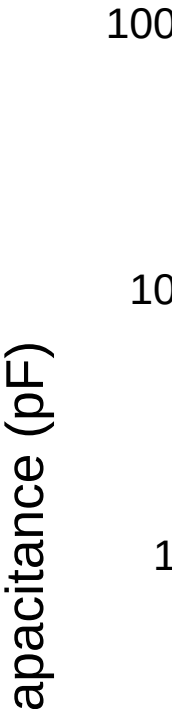
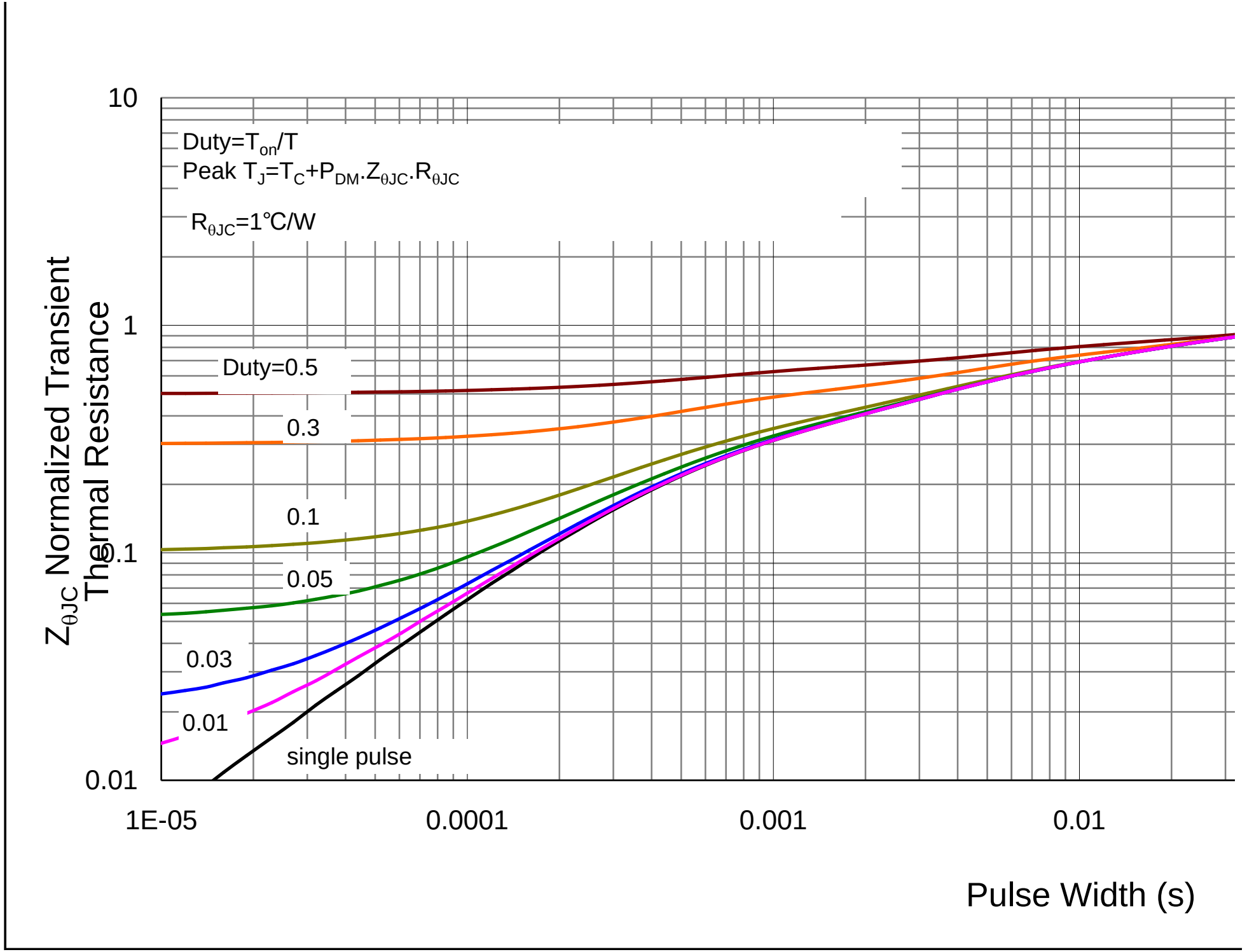
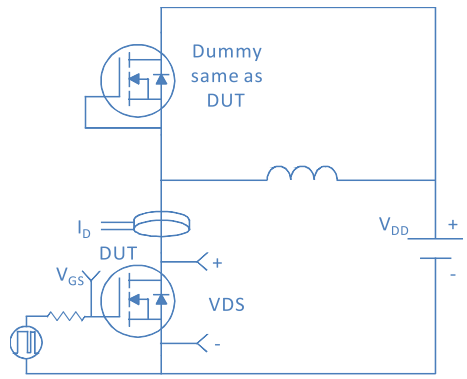


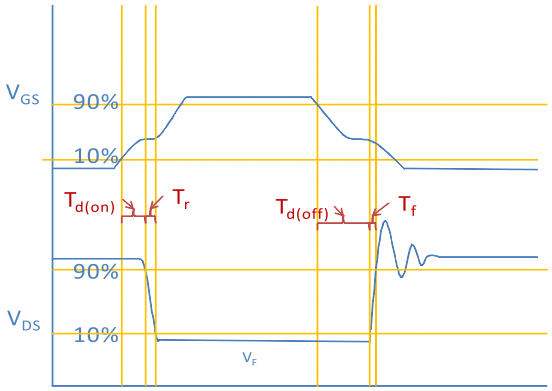
Figure 8.



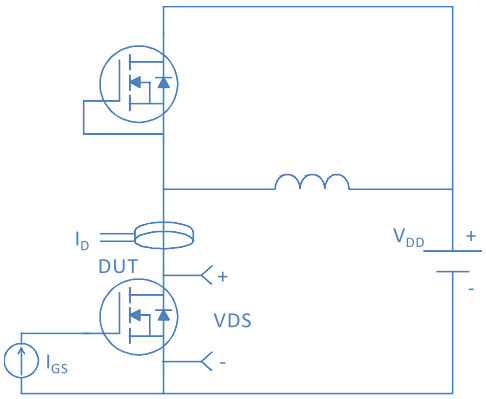

10
1
0.1
0.01
Duty=T_{on}/T
Peak T_J=T_C+P_{DM}.$Z_{\theta JC}$.$R_{\theta JC}$
$R_{\theta JC}$=1℃/W
Duty=0.5
0.3
0.1
0.05
0.03
0.01
single pulse
$Z_{\theta JC}$ Normalized Transient Thermal Resistance
1E-05
0.0001
0.001
0.01
Pulse Width (s)

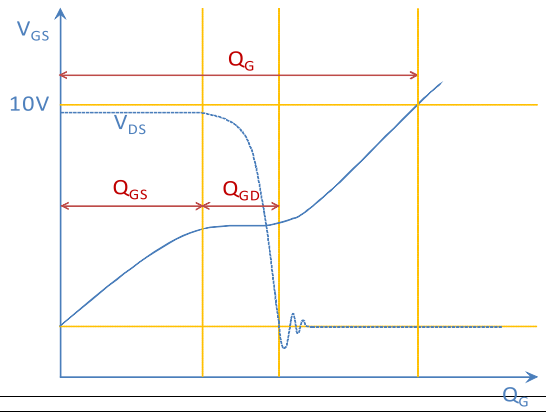
Inductive switching Test



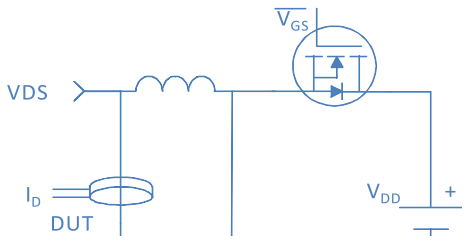


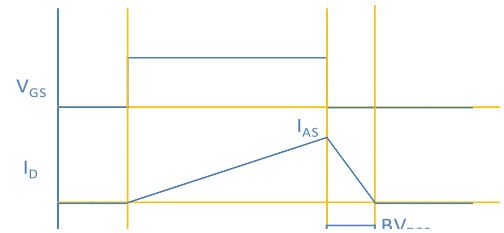
Gate Charge Test

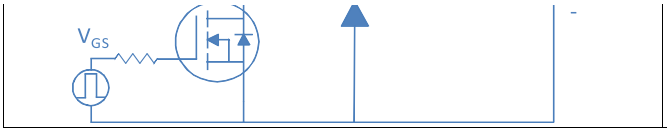


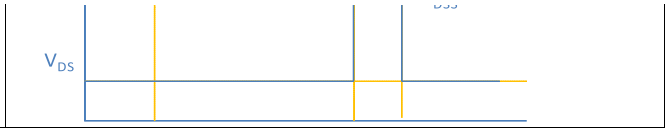


Uclamped Inductive Switching (UIS) Test

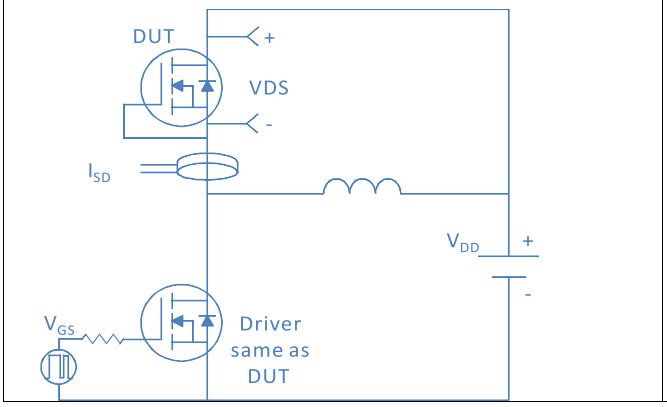


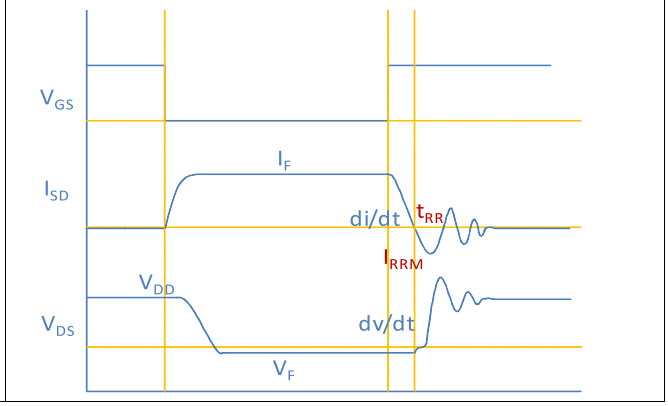






Diode Recovery Test





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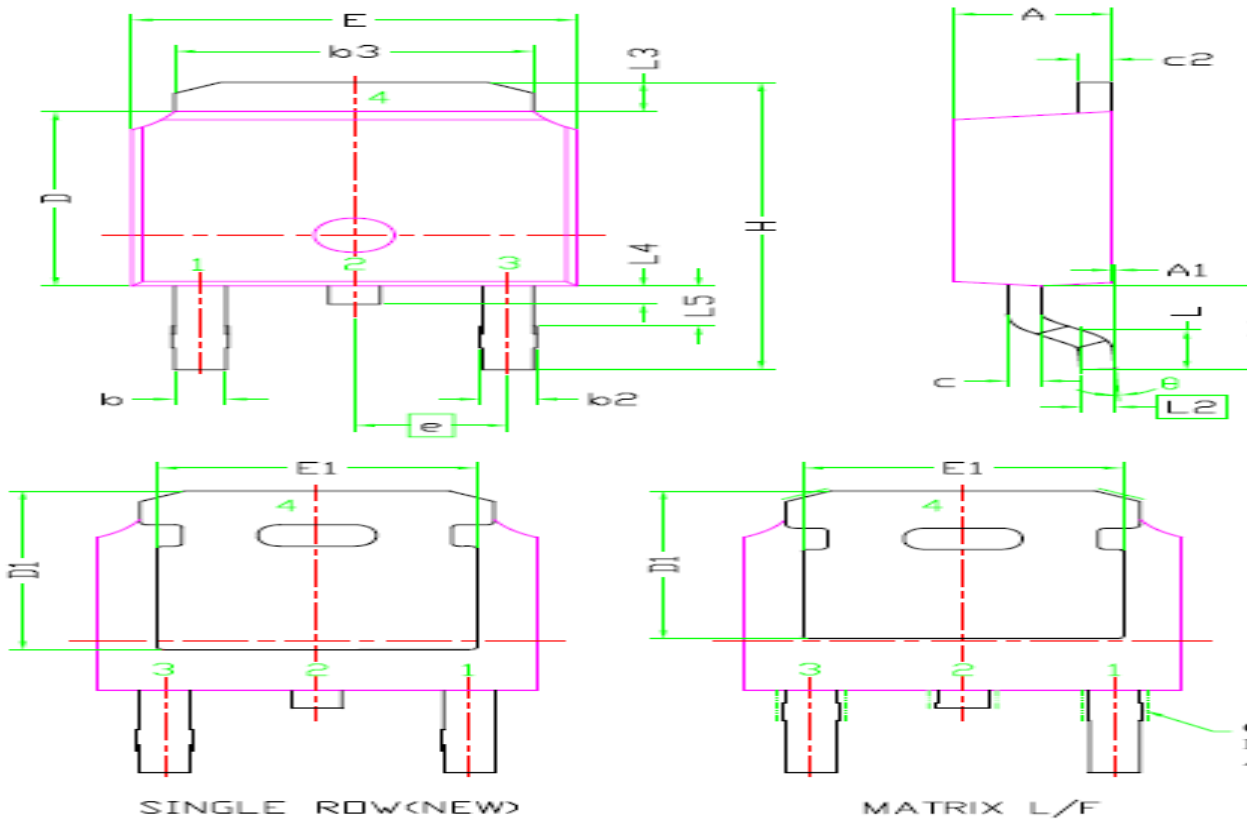
E
b3
L3
4
D
H
L4
L5
1
2
3
b
b2
e
A
c2
A1
L
c
θ
L2
E1
D1
SINGLE ROW(NEW)
MATRIX L/F